IJARETY

International Journal of Advanced Research in Education and TechnologY (IJARETY)

Volume 11, Issue 1, January- February 2024

Impact Factor: 7.394

www.ijarety.in editor.ijarety@gmail.com

International Journal of Advanced Research in Education and TechnologY(IJARETY)

| ISSN: 2394-2975 | www.ijarety.in| | Impact Factor: 7.394| A Bi-Monthly, Double-Blind Peer Reviewed & Referred Journal |

|| Volume 11, Issue 1, January-February 2024 ||

Design of Low-Power D-Flip-Flop using Redundant Pre-Charge Free Technique

Dr. P. Rama Krishna[1], Dr. T. Rajesh[2], M. Muralikrishna[3] M. Swathi[4]

Assistant Professor, Department of ECE, Anurag University, Hyderabad, India[1]

Associate Professor, Department of ECE, Anurag University, Hyderabad, India[2]

Assistant Professor, Department of ECE, Anurag University, Hyderabad, India[3,4]

ABSTRACT: As basic components, optimizing power consumption of flip-flops (FFs) can significantly reduce the power of digital systems. In this article, an energy-efficient retentive true single- phase-clocked (TSPC) FF is proposed. With the employment of input-aware pre-charge scheme, the proposed TSPC FF pre-charges only when necessary. In addition, floating node analysis and transistor level optimization are employed to further ensure the high energy efficiency of the FF without significantly increasing the area. The simulations based on 45- nm CMOS technology show that at a supply voltage of 1 V, the power consumption of the proposed FF is expected 84.37% lower than that of conventional transmission-gate flip-flop (TGFF) at 10% data activity.

I. INTRODUCTION

As basic components, optimizing power consumption of flip-flops (FFs) can significantly reduce power of digital systems. In this article, an energy-efficient retentive truesingle- phase-clocked TSPC) FF is proposed. With the employment of input-aware precharge scheme, the proposed TSPC FF precharges only when necessary. In addition, floating node analysis and transistor level optimization are employed to further ensure the high energy efficiency of the FF without significantly increasing the area. Measurement results of ten test chips demonstrate the great energy efficiency of the proposed FF. Furthermore, the CK-to-Q delay of the proposed FF is 26.18% lower than that of TGFF at a supply voltage of 1 V. **W**ITH the development of the process, the performance of digital system is greatly improved, and the power consumption is becoming an important limitation of digital systems. In addition, with the rapid development of the Internet of Things (IoT), IoT devices are deployed on a large scale In such battery-powered or self-powered devices, low-power design becomes the focus of attention

As basic components, the power of flip-flops (FFs) accounts for a large part of the power of digital systems Therefore, reducing the power consumption of FFs can significantly reduce the power consumption of the digital systems. Voltage-scaling technique has been proved to be an attractive method to decrease the power consumption of digital systems In order to obtain the power benefits of voltage-scaling technique, it is necessary to design an FF capable of operating at both and near/subthreshold supply voltage. The transmission-gate flip-flop (TGFF) is the most widely used FF in current digital systems. The schematic of TGFF is shown in Fig. 1. The TGFF is a -free FF which is suitable for near-threshold operation. The main drawback of TGFF is the network. The internal nodes CKN and CKI toggle no matter what the input data is, and the nodes CKN and CKI drive a larger number of transistors. Thus, the power consumption of TGFF is still large even if the data activity remains low. To reduce the power consumption of FF, the use of complementary clock signals should be optimized.

Many low-power single-phase-clocked FFs have been proposed in previous works But there are still some problems that affect the power consumption of these FFs. For example, some of the FFs fail at low supply voltage and some suffer from large precharge power In order to solve these problems, a low power true-single-phase-clocked (TSPC) FF is proposed in this article. The FF is contention-free and suitable for wide supply voltage operation. Furthermore, redundant operation is totally removed in the proposed FF and the power consumption is further optimized compared with previous low-power FFs.Flip Flop (FF) contributes as a major element in power consumption as its latch structure undergoes number of redundant transitions and alternative charging and discharging in internal node. Low power flip flop design is very much essential for an efficient design of low power digital systems since it is the basic storage element of major digital designs.

Flip flops and latches consume a large amount of power due to superfluous transitions and clocking system. The Clock (Clk) distribution network and flip flops together contribute 30% to 60% of total power dissipation in a system. A flipflop with high performance and power efficiency is possible only by a better design.The power consumption should be reduced considerably or resulting heat will limit the feasible package and performance of VLSI systems (Rasouli et

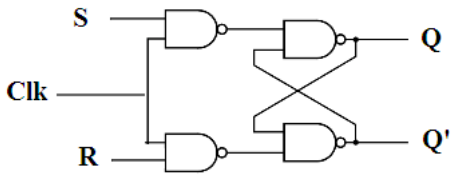
| ISSN: 2394-2975 | www.ijarety.in| | Impact Factor: 7.394| A Bi-Monthly, Double-Blind Peer Reviewed & Referred Journal |

|| Volume 11, Issue 1, January-February 2024 ||

al. 2005). Flip flops are the critical timing elements which have a massive impact on the circuit area, power consumption and speed (Mahmoodi et al. 2009). An efficient method to reduce power is to reduce the switching activity by eliminating redundant data in transition. Pulsed flip flops which has single-latch structure and less redundant switching activity is moreadmired than the conventional Transmission Gate (TG) and master slave based flip flops in low power and high-speed applications (Jin Fa lin 2013). Gate Diffusion Input (GDI) based flip flops are preferred (Arkaidy et al. 2009) for reduced area and power consumption. The energy used by clock distribution network is steadily steeping up and has become a superior fraction of the integrated circuit power (Jin fa Lin 2013). Power Consumption is calculated by multiple factors like frequency, supply voltage, capacitance, leakage current, data activity and short circuit current. It is given by the expression

P= Pdynamic + Pshort circuit + Pleakage
In the equation , Pdynamic is power due to switching activities. P short circuit is the short circuit power resulting from finite rise and fall time of input signals leading to pull up and pull down network to be ON for a short span of time.
Pshort circuit = Ishort circuit * Vdd
Pleakage is the leakage power. The reduction in supply voltage leads to decrease in the threshold voltage in order to maintain performance. However, this gives rise to the exponential growth of the subthreshold leakage current
.Pleakage current = Ileakage current * Vdd
Flip flop and its typesf

flip flop is an electronic circuit which stores a logical level data input signals corresponding to the clock pulse. The main disparity between latches and flip flops is that the output of the latches will be constantly affected by the input as long as the enable pin is active. In case of flip flops, the data change only at the arrival of positive or negative edge of the clock. The flip flop content remains unchanged even at change in input after rising or falling edge. There are four types of flip flops. They are:i) SR(Set Reset) flip flopii) D (Delay or Data) flip flopiii) JK (Jack Kilby) flip flopiv) T (Toggle) flip flopThe Characteristic equation, truth table, excitation table and logic diagram are presented in the following section.1.1.1 SR Flip FlopSR flip flops are useful in control applications where set or reset of the data bit plays a key role. However, SR flip-flops change their stored values only at the active edge or level of the clock signal. The main drawback of SR flip-flops is that it enters into an undefined state when both inputs are made high simultaneously. The structure of SR flip flop is given in Figure 1.1



SR flip flop

The state diagram, Characteristic equation and symbol of SR flip flop is represented in Figure 1.2 State diagram and symbol of SR Flip flopThe truth table of the SR flip flop is tabulated in table 1.1. It is clearly evident that the flip flop enters into indeterminate state when S=1 and R=1.1.1.2 D Flip FlopD-Flip flops are the fundamental building blocks of major VLSI systems because of its ability to capture data with respect to the clock signal. The data will be retained in the flip flop until the arrival of next clock and other input changes will be ignored. D-flip flops are called as data flip flop due to its ability to latch and remember data. D-Flip flops are also termed as delay flip flop because the above mentioned latching and remembering task helps in creating delay so as to process the data in high level architectures.
D-flip flops are the modification of SR flip flops with an additional inverter to avoid indeterminate state produced by the SR flip flops. The S and R inputs of the SR flip flop are replaced by a single input D. The structure of D flip flop is given in Figure 1.3 The state diagram, Characteristic equation and symbol of D flip flop is represented in Figure 1.4.1.3 JK Flip FlopJK flip flops circuit design is similar to that of SR flip flops. The J input is same as the S input as it sets the flip-flop. Similarly, the K input is same as the R input which resets the flip flop. The major difference is when both inputs are made high, the next state of the JK flip flop is inverse of the current whereas SR

| ISSN: 2394-2975 | www.ijarety.in| | Impact Factor: 7.394| A Bi-Monthly, Double-Blind Peer Reviewed & Referred Journal |

|| Volume 11, Issue 1, January-February 2024 ||

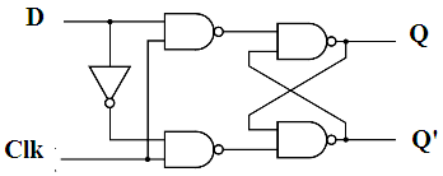
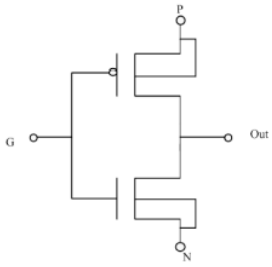


Figure 2 Structure of D flip flop

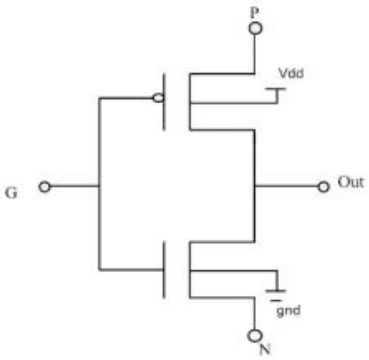
Overview of GDI approach

This section gives a brief overview on one of the popular digital logic techniques in recent times, Gate-Diffusion Input . Number of complex logic functions can be realised using GDI technique with only two transistors. The GDI logic depends on the use of a simple cell as shown in Fig. 1. The structure of the cell resembles the static CMOS inverter but there are some key differences to note. GDI cell comprises of 3-inputs: G-common input to both PMOS and NMOS, N-input to the source/drain of the NMOS and Pinput to the source/drain of the PMOS.Body terminals of both the NMOS and PMOS are arbitrarily biased in GDI by connecting to the inputs N and P, respectively. The GDI methodology was originally introduced for fabrication in Silicon on Insulator (SOI) and twin-well CMOS processes.

Later, standard CMOS compatible GDI cell was introduced it was shown that most of the logic functions like AND, OR, XOR, and MUX are complex which require 6–12 transistors to implement using conventional static CMOS and transmission gate logic, but the same logic functions can be implemented with only two transistors using GDI cell by simply changing the inputs. Table 1 shows the logic table for implementing various boolean functions using GDI and Table 2 shows the transistor count comparison between the GDI and conventional CMOS implementations of different Boolean functions. F1 and F2 are the two universal logic functions offered by GDI which can be used to realise other complex functions more efficiently than th universal NAND and NOR logic gates.



a



b

Fig: 3 Structure of a basic gate diffusion input (GDI) cell with inputs G, P, and N.

| ISSN: 2394-2975 | www.ijarety.in| | Impact Factor: 7.394| A Bi-Monthly, Double-Blind Peer Reviewed & Referred Journal |

|| Volume 11, Issue 1, January-February 2024 ||

II. PROPOSED SYSTEM

The TSPC FF pre-charges only when necessary. In addition, floating node analysis and transistor level optimization are employed to further ensure the high energy efficiency of the FF without significantly increasing the area. The simulations based on 45- nm CMOS technology show that at a supply voltage of 1 V, the power consumption of the proposed FF is expected 60% lower than that of conventional transmission-gate flip-flop (TGFF) at 10% data activity.

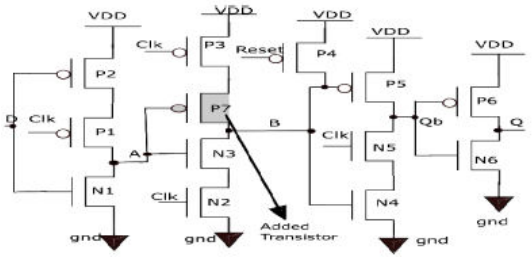


Fig 4: Positive edge triggered MTSPC DFF

Analysis of the behavior of node B reveals that for the times, when there is a path to ground, node B will always pre-charged to HIGH when clock (Clk) is LOW and will return back to LOW when Clk is HIGH. So, whenever the input D is at a stable LOW for a long time with respect to Clk, node B experiences continuous toggling. Such unnecessary behavior not only accounts for large power consumption but is also a source of noise on the output node, Q, caused by erroneous glitches caused every time Clk makes a LOW-to-HIGH transition. To solve this problem, the proposed MTSPC DFF architecture reveals that whenever the path to ground is ON, pre-charging node B should be suspended to prevent toggling. A simple technique that works here is to add a PMOS transistor that prevents the pre-charging phase to occur without affecting the global operation of the flip-flop. To prove this claim, consider the above Fig.In this section the existing positive edge triggered TSPC DFF and the proposed positive edge triggered MTSPC DFF are presented. The proposed MTSPC DFF is not only consumed low power but also it has a higher maximum frequency of oscillation and PDP compared to TSPC DFF, as we will discuss shortly.A. Operation of the existing TSPC DFFIn the existing positive edge triggered TSPC D Flip-Flop in the Fig., when the clock signal Clk is LOW, the input is isolated from the output Qb, since the node B pre-charged to HIGH, and Qb maintains its older value.

When Clk is HIGH, node B will not be affected. Therefore when Clk is stable at either HIGH or LOW, the input is isolated from the output. When Clk makes a LOW-to-HIGH transition, the Qb will latch the complement of the input and Q will pass the input to the output. When the preset input (RESET) is LOW the preset PMOS will be ON and Qb maintains its value HIGH as long as RESET is LOW.Operation of the proposed MTSPC DFFAnalysis of the behavior of node B reveals that for the times, when there is a path to ground, node B will always precharged to HIGH when clock (Clk) is LOW and will return back to LOW when Clk is HIGH. So, whenever the input D is at a stable LOW for a long time with respect to Clk, node B experiences continuous toggling. Such unnecessary behavior not only accounts for large power consumption but is also a source of noise on the output node, Q, caused by erroneous glitches caused every time Clk makes a LOW-to-HIGH transition. To solve this problem, the proposed MTSPC DFF architecture reveals that whenever the path to ground is ON, pre-charging node B should be suspended to prevent toggling. A simple technique that works here is to add a PMOS transistor that prevents the pre-charging phase to occur without affecting the global operation of the flip-flop.

To prove this claim, consider the following Fig. 3. If Clk is LOW and D is LOW, node B, and consequently the node Qb, maintain their old values. If D changes to HIGH,node B pre-charge to HIGH; again, the output remains unaffected. Now, if Clk makes a LOW-to-HIGH transition, node B maintains its charge (HIGH), and the node becomes LOW. After that, even if D becomes LOW again, the output will not be affected. If Clk makes a LOW-to-HIGHtransition while D is LOW, node B will discharge, and the node Qb will be HIGH and Q will be low. Whenever the preset input (RESET) is low the preset PMOS will ON and the node Qb maintains HIGH. The simulation results of this preset-able MTSPC D flip-flop is shown Fig. 4 and in this regard we were used CADENCE Virtuoso 45nm CMOS technology tool with clock frequency 1GHz and simulation times of 10nS.

The power consumed by MTSPC D flip-flop is11.83 µW.C. Toggle mode Operation of the TSPC and MTSPC DFFTo test the toggle mode of operation, the output, Qb is connected to D input of the TSPC and MTSPC D flip-flop. The clock frequency applied for toggle mode operation is 2 GHz for TSPC and 4 GHz for MTSPC DFF. The simulation results of toggle mode TSPC DFF with clock frequency of 2 GHz and simulation time of 10 ns is shown in Fig. 5 and

| ISSN: 2394-2975 | www.ijarety.in| | Impact Factor: 7.394| A Bi-Monthly, Double-Blind Peer Reviewed & Referred Journal |

|| Volume 11, Issue 1, January-February 2024 ||

the simulation results of toggle mode MTSPC DFF with clock frequency of 4 GHz and simulation time of 10 ns is shown in Fig

III. RESULTS

In order to analyze the performance of the proposed circuit CADENCE simulations were carried out based on 45nm and technologies, and its performance have been compared with the other DFFs. The operating frequency of all the DFF is set at 10MHz. The average power consumption, evaluated. The average power consumption is average value of circuit power consumption under consideration of all the possible input combinations and several cycles. Clearly, the DFF has the least power consumption at all varying supply voltages among other DFF. It is apparent that the CMOS has the smallest delay at lower supply voltage.

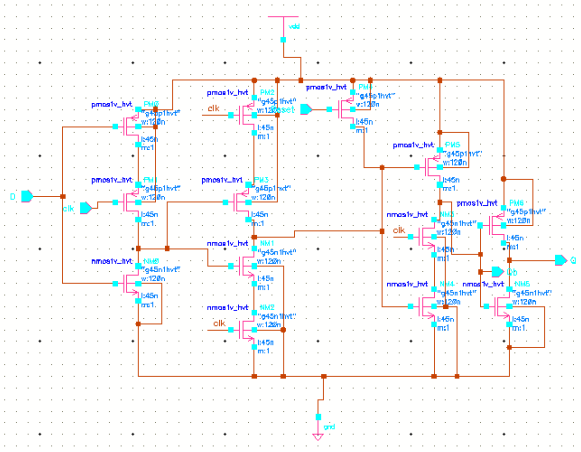


Fig5: Schematic of the proposed DFF

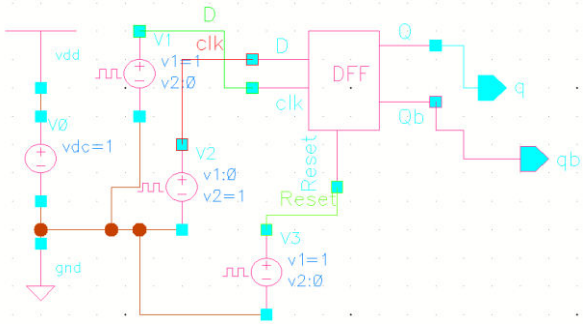


Fig6: Test bench of the proposed DFF

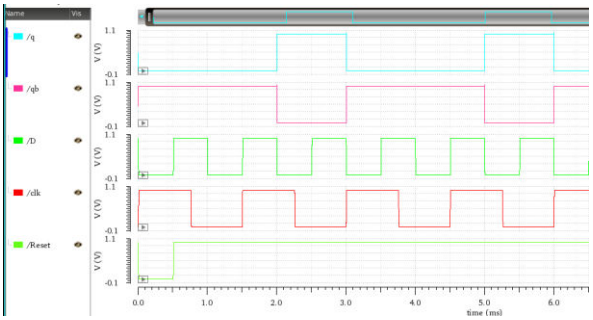


Fig7: Simulation results of DFF

| ISSN: 2394-2975 | www.ijarety.in| | Impact Factor: 7.394| A Bi-Monthly, Double-Blind Peer Reviewed & Referred Journal |

|| Volume 11, Issue 1, January-February 2024 ||

Table1 : Performance Comparison

Parameters	TSPC	This work
Input clock frequency	1Mz	10Mz
Clock-to-Q delay (Lowto-High)	92ps	61ps
Clock-to-Q delay (Highto Low)	143ps	102ps
Average Clock-to-Q Delay	128ps	71ps
Average power consumption	65uw	16uw

IV. CONCLUSION

In this work, a new preset-able modified true single phase clocked (MTSPC) D flip-flop with GDI technique is proposed. The technique utilizes a clocked dynamic logic. The unlike a TSPC D flip-flop. The preset-able TSPC D flip-flop has more noise at the output, this noise not only affect the output but also consumed very large power. The Proposed preset-able MTSPC D flip-flop has very less noise at the output and consequently the power consumption is also very low. The proposed preset-able MTSPC D flip-flop can be use fast, low power electronics world. Using the above technique a DFF is designed using 4nm CMOS technology. In this design maximum 10MHz frequency of operation is achieved. Power consumption is reduced from 20 uW

REFERENCES

1. Abdelkader, O, Mostafa, H, Abdelhamid, H & Soliman, A 2015,'Impact of technology scaling on the minimum energy point forFinFET based flip-flops', Proceedings of the IEEE InternationalConference on Electronics, Circuits, and Systems, pp. 462-465.
2. Absel, K, Manuel, L & Kavitha, RK 2013, 'Low-power dual dynamicnode pulsed hybrid flip-flop featuring efficient embedded logic', IEEEtransactions on very large scale integration (VLSI) systems, vol. 21, no.9, pp. 693-1704.
3. Aditya, KVSS, Kotaru, BB & Naik, BB 2014, 'Design of low powershift register using activity-driven optimized clock gating and run-timepower gating', Proceedings of the IEEE International Conference onCommunication and Electrical Engineering, pp. 1-7.
4. Alioto, M , Consoli, E & Palumbo, G 2015, 'Comparative analysis ofthe robustness of master-slave flip-flops against variations, Proceedingsof the IEEE International Conference on Electronics, Circuits, andSystems, pp. 117-120.
5. Alioto, M, & Palumbo, G 2003, 'Design of MUX, XOR and D-latchSCL gates', Proceedings of the IEEE International Symposium onCircuits and Systems, Vol. 5, pp. V261-V264.
6. Alioto, M, Consoli, E & Palumbo, G 2014, 'Analysis and comparisonof variations in double edge triggered flip-flops', Proceedings of theIEEE 5th European Workshop on CMOS Variability , pp. 1-6.
7. Alioto, M, Palumbo, G & Consoli, E 2015, 'PVT variations indifferential flip-flops: A comparative analysis', Proceedings of theIEEE European Conference on Circuit Theory and Design, pp. 1-4.
8. Aloisi, W & Mita, R 2008, 'Gated-clock design of linear-feedback shiftregisters', IEEE Transactions on circuits and systems II: Express briefs,vol. 55, no. 6, pp. 546-550.
9. Ananthi, M & Kumar, CS 2015, 'QDR SRAM Design Using Multi-bitFlip-Flop', International Journal of Advanced Research in Electronicsand Communication Engineering, vol. 4, no. 3, pp. 614-618.
10. Arunya, R, Ramya, A, Umarani, P & Balamugaran, V 2013, 'Design Of3 bit synchronous Counter using DLDFF', International Journal ofEngineering Research and Applications, vol. 3, no. 2, pp.1258-1262.
11. Ashna, VR & Jagadeeswari, M 2013, 'Design of low power clockingsystem using merged flip-flop technique', Proceedings of the IEEEInternational Conference on Computer Communication andInformatics, pp. 1-6.
12. Ashwini, H, Rohith, S & Sunitha, KA 2016, 'Implementation of highspeed and low power 5T-TSPC D flip-flop and its application',Proceedings of the IEEE International Conference on Communicationand Signal Processing, pp. 275-279.
13. Balan, S & Daniel, SK 2012, 'Dual-edge triggered sense-amplifier flipflopfor Low Power systems', Proceedings of the IEEE InternationalConference on Green Technologies, pp. 135-142.
14. Berg, Y 2011, 'Novel high speed differential CMOS flip-flop for ultralow-voltage appications', Proceedings of the IEEE 9th InternationalConference on New Circuits and Systems, pp. 241-244.
15. Bernard, S, Valentian, A, Belleville, M, Bol, D & Legat, JD 2013, 'Anefficient metric of setup time for pulsed flip-flops based on outputtransition time', Proceedings of the IEEE International Conference onIC Design & Technology, pp. 9-12.

International Journal of Advanced Research in Education and Technology

ISSN: 2394-2975

Impact Factor: 6.421

www.ijarety.in editor.ijarety@gmail.com